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ATTORNEY DOCKET NO. 035905-0118

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4-2502
JC628 U.S. PTO
10/06/02
02/05/02

Applicant: Igor G. KOUZNETSOV et al.

Title: TWO MASK FLOATING GATE EEPROM AND METHOD
OF MAKING

Appl. No.: Unassigned

Filing Date: 02/05/2002

Examiner: Unassigned

Art Unit: Unassigned

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO/SB/08B is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

Appl. No. Unassigned

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), within three (3) months of the filing date of the application.

RELEVANCE OF EACH DOCUMENT

All of the documents are in English.

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08B be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

February 5, 2002
Date

FOLEY & LARDNER
Customer Number: 22428



22428

PATENT TRADEMARK OFFICE

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Reg. No. 35,264

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	Unassigned
Date Submitted: February 5, 2002				Filing Date	02/05/2002
(use as many sheets as necessary)				First Named Inventor	Igor KOUZNETSOV et al.
Sheet	1	of	7	Group Art Unit	Unassigned
				Examiner Name	Unassigned
				Attorney Docket Number	035905-0118

#2/5/02
S-376
02/05/02

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
A1	5,427,979			Chang	06/27/1995	
A2	5,070,384			McCollum et al.	12/03/1991	
A3	4,498,226			Inoue et al.	02/12/1985	
A4	4,489,478			Sakurai	12/25/1984	
A5	4,272,880			Pashley	06/16/1981	
A6	4,646,266			Ovshinsky et al.	02/24/1987	
A7	5,835,396			Zhang	11/10/1998	
A8	5,745,407			Levy et al.	04/28/1998	
A9	5,535,156			Levy et al.	07/09/1996	
A10	5,306,935			Esquivel et al.	04/26/1994	
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A42	5,776,810			Guterman et al.	07/07/1998	
A43	5,835,396			Zhang	11/10/1998	

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				Attorney Docket Number	035905-0118

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		U.S. Patent Document		
A44	5,883,409		Guterman et al.	03/16/1999
A45	6,034,882		Johnson et al.	03/07/2000
A46	3,629,863		Neale	12/21/1971
A47	3,571,809		Nelson	03/23/1971
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A65	4,876,220		Mohsen et al.	10/24/1989
A66	3,671,948		Cassen et al.	06/20/1972
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A68	5,978,258		Manning	11/02/1999

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
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	A69	JOHN H. DOUGLAS: "The Route to 3-D Chips," High Technology, September 1983, pgs. 55-59, Vol. 3, No. 9, High Technology Publishing Corporation, Boston, MA		
	A70	M. ARIENZO et al.: "Diffusion of Arsenic in Bilayer Polycrystalline Silicon Films," J. Appl. Phys., January 1984, pgs. 365-369, Vol. 55, No. 2, American Institute of Physics		

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	A71	O. BELLEZZA et al.: "A New Self-Aligned Field Oxide Cell for Multimegabit Eproms," IEDM, pgs. 579-582, IEEE		
	A72	S.D. BROTHERTON et al.: "Excimer-Laser-Annealed Poly-Si Thin-Film Transistors," IEEE Transactions on Electron Devices, February 1993, pgs. 407-413, Vol. 40, No. 2, IEEE		
	A73	P. CANDELIER et al.: "Simplified 0.35-μm Flash EEPROM Process Using High-Temperature Oxide (HTO) Deposited by LPCVD as Interpoly Dielectrics and Peripheral Transistors Gate Oxide," IEEE Electron Device Letters, July 1997, pgs. 306-308, Vol. 18, No. 7, IEEE		
	A74	MIN CAO et al.: "A High-Performance Polysilicon Thin-Film Transistor Using XeCl Excimer Laser Crystallization of Pre-Patterned Amorphous Si Films," IEEE Transactions on Electron Devices, April 1996, pgs. 561-567, Vol. 43, No. 4, IEEE		
	A75	MINO CAO et al.: "A Simple EEPROM Cell Using Twin Polysilicon Thin Film Transistors," IEEE Electron Device Letters, August 1994, pgs. 304-306, Vol. 15, No. 8, IEEE		
	A76	BOMY CHEN et al.: "Yield Improvement for a 3.5-ns BICMOS Technology in a 200-mm Manufacturing Line," IBM Technology Products, 1993, pgs. 301-305, VLSITSA		
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	A78	BOAZ EITAN et al.: "Alternate Metal Virtual Ground (AMG) - A New Scaling Concept for Very High-Density EPROM's," IEEE Electron Device Letters, pgs. 450-452, Vol. 12, No. 8, August 1991, IEEE		
	A79	BOAZ EITAN et al.: "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," IEEE Electron Device Letters, pgs. 543-545, Vol. 21, No. 11, November 2000, IEEE		
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	A81	DR. HEINRICH ENDERT: "Excimer Lasers as Tools for Material Processing in Manufacturing," Technical Digest: International Electron Devices Meeting, 1985, pgs. 28-29, Washington, DC, December 1-4, 1985, Göttingen, Germany		
	A82	DOV FROHMAN-BENTCHKOWSKY: "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, pgs. 301-306, Vol. sc-6, No. 5, October 1971		
	A83	G.K. GIUST et al.: "Laser-Processed Thin-Film Transistors Fabricated from Sputtered Amorphous-Silicon Films," IEEE Transactions on Electron Devices, pgs. 207-213, Vol. 47, No. 1, January 2000, IEEE		
	A84	G.K. GIUST et al.: "High-Performance Thin-Film Transistors Fabricated Using Excimer Laser Processing and Grain Engineering," IEEE Transactions on Electron Devices, pgs. 925-932, Vol. 45, No. 4, April 1998, IEEE		

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	A85	G.K. GIUST et al.: "High-Performance Laser-Processed Polysilicon Thin-Film Transistors," IEE Electron Device Letters, pgs. 77-79, Vol. 20, No. 2, February 1999, IEEE		T ⁶
	A86	C. HAYZELDEN et al.: "Silicide Formation and Silicide-Mediated Crystallization of Nickel-Implanted Amorphous Silicon Thin Films," J. Appl. Phys. 73(12), June 15, 1993, pgs. 8279-8289, 1993 American Institute of Physics		
	A87	FUMIHIKO HAYASHI et al.: "A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pgs. 87-88, Stanford University, Stanford, CA 94305, USA		
	A88	STEPHEN C.H. HO et al.: "Thermal Stability of Nickel Silicides in Different Silicon Substrates," Department of Electrical and Electronic Engineering, pgs. 105-108, 1998, IEEE		
	A89	SUNG-HOI HUR et al.: "A Poly-Si Thin-Film Transistor EEPROM Cell with a Folded Floating Gate," IEEE Transactions on Electron Devices, pgs. 436-438, Vol. 46, No. 2, February 1999, IEEE		
	A90	J. ESQUIVEL et al. "High Density Contactless, Self Aligned EPROM Cell Array Technology," Texas Instruments (Dallas), IEDM 86, pgs. 592-595, 1986, IEEE		
	A91	R. KAZEROUNIAN et al.: Alternate Metal Virtual Ground EPROM Array Implemented in a 0.8µm Process for Very High Density Applications," IEDM 91, pgs. 311-314, 1991, IEEE		
	A92	CHANG-DONG KIM et al.: "Short-Channel Amorphous-Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, pgs. 2172-2176, Vol. 43, No. 12, December 1996, IEEE		
	A93	JOHAN H. KLOOTWIJK et al.: "Deposited Inter-Polysilicon Dielectrics for Nonvolatile Memories," IEEE Transactions on Electron Devices , pgs. 1435-1445, Vol. 46, No. 7, July 1999, IEEE		
	A94	NEC Corporation: "A Novel Cell Structure for Giga-bit EPROMs and Flash Memories Using Polysilicon Thin Film Transistors," 1992 Symposium on VLSI Technology Digest of Technical Papers, pgs. 44-45, 1992, IEEE		
	A95	WEBPAGE-JA-HUM KU et al.: "High Performance pMOSFETs With Ni(Si/ _x Ge/ _{1-x})Si/Sub 0.8/Ge/ _{0.2} / gate, IEEE Xplore Citation," VLSI Technology, 200. Digest of Technical Paper Symposium on page(s): 114-115 June 13-15 2000		
	A96	NAE-IN LEE et al.: "High-Performance EEPROM's Using N- and P-Channel Polysilicon Thin-Film Transistors with Electron Cyclotron Resonance N ₂ O-Plasma Oxide," pgs. 15-17, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IEEE		
	A97	JIN-WOO LEE et al.: "Improved Stability of Polysilicon Thin-Film Transistors under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel," IEEE Electron Device Letters, 1998, pgs. 265-268, IEEE		

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	A98	SEOK-WOON LEE et al.: "Pd induced lateral crystallization of Amorphous Si Thin Films," Appl. Phys. Lett. 66 (13), pgs. 1671-1673, 27 March 1995, American Institute of Physics		
	A99	K. MIYASHITA et al.: "Optimized Halo Structure for 80 nm Physical Gate CMOS Technology with Indium and Antimony Highly Angled Ion Implantation," IEDM 99-645, pgs. 27.2.1-27.2.4, 1999, IEEE		
	A100	N.D. YOUNG et al.: "The Fabrication and Characterization of EEPROM Arrays on Glass Using a Low-Temperature Poly-Si TFT Process," IEEE Transactions on Electron Devices, pgs. 1930-1936, Vol. 43, No. 11, November 1996, IEEE		
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	A103	NORIAKI SATO et al.: "A New Programmable Cell Utilizing Insulator Breakdown," IEDM, 1985 pages 639-642, IEEE		
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	A105	SEUNGHEON SONG et al.: "High Performance Transistors with State-of-the-Art CMOS Technologies," IEDM 99, pgs. 427-430, 1999, IEEE		
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	A107	YOSHIHIRO TAKAO et al." "Low-Power and High-Stability SRAM Technology Using a Laser-Recrystallized p-Channel SOI MOSFET," IEEE Transactions on Electron Devices, pgs. 2147-2152, Vol. 39, No. 9, September 1992, IEEE		
	A108	KENJI TANIGUCHI et al.: "Process Modeling and Simulation: Boundary Conditions for Point Defect-Based Impurity Diffusion Model," IEEE Transactions on Computer-Aided Design , pgs. 1177-1183, Vol. 9, No. 11, November 1990, IEEE		
	A109	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, pgs. 391-393, Vol. 21, No. 9, September 2000, IEEE		

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.		
	A110	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, Vol. 21, No. 9, pgs. 439-441, September 2000, IEEE		T ⁶
	A111	HONGMEI WANG et al.: "Super Thin-Film Transistor with SOI CMOS Performance Formed by a Novel Grain Enhancement Method," IEEE Transactions on Electron Devices, pgs. 1580-1586, Vol. 47, No. 8, August 2000, IEEE		
	A112	MARVIN H. WHITE et al. "On the Go With Sonos," Circuit & Devices, pgs. 22-31, July 2000, IEEE		
	A113	B.J. WOO et al.: "A Novel Memory Cell Using Flash Array Contactless Eprom (Face) Technology," IEDM, pgs. 90-93, 1990, IEEE		
	A114	WEBPAGE - QI XIANG et al.: "Deep sub-100 nm CMOS with Ultra Low Gate Sheet Resistance by NiSi," VLSI Technology, 2000. Digest of Technical Paper Symposium on... pgs. 76-77, IEEE Xplore, June 13-15, 2000		
	A115	QI XIANG et al."Deep Sub-100nm CMOS with Ultra Low Gate Sheet Resistance by NiSi," IEEE, pgs. 76-77, 2000, Symposium on VLSI Technology Digest of Technical Papers		
	A116	QIUXIA XU et al.: "New Ti-SALICIDE Process Using Sb and Ge Preamorphization for Sub-0.2 μm CMOS Technology," IEEE Transactions on Electron Devices, pgs. 2002-2009, Vol. 45, No. 9, September 1998, IEEE		
	A117	KUNIYOSHI YOSHIKAWA et al.: "An Asymmetrical Lightly Doped Source Cell for Virtual Ground High-Density EPROM's," IEEE Transactions on Electron Devices, pgs. 1046-1051, Vol. 37, No. 4, April 1990, IEEE		
	A118	VIVEK SUBRAMANIAN: "Control of Nucleation and Grain Growth in Solid-Phase Crystallized Silicon for High-Performance Thin Film Transistors," A Dissertation Submitted to the Department of Electrical Engineering and the Committee of Graduate Studies of Stanford University in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy, June 1998		
	A119	BRIAN DIPERT: "Exotic Memories, Diverse Approaches," EDN Asia, September 2001		
	A120	JOHN R. LINDSEY et al.: "Polysilicon Thin Film Transistor for Three Dimensional Memory," The 198 th Meeting of The Electrochemical Society, Volum 2000-2		
	A121	DIETMAR GOGL et al.: "A 1-Kbit EEPROM in SIMOX Technology for High-Temperature Applications up to 250° C," IEEE Journal of Solid-State Circuits, October 2000, Vol. 35, No. 10, IEEE		
	A122	STANLEY WOLF: "Silicon Processing for the VLSI Era," Semiconductor Memory Process Integration, Volume 2		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	Unassigned
Date Submitted: February 5, 2002 <i>(use as many sheets as necessary)</i>				Filing Date	02/05/2002
				First Name Inventor	Igor KOUZNETSOV et al.
				Group Art Unit	Unassigned
				Examiner Name	Unassigned
Sheet	7	of	7	Attorney Docket Number	035905-0118

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Number	Kind Code ² (if known)		
	A123	5,383,149		Hong	01/17/1995
	A124	5,572,046		Takemura	11/05/1996

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	A125	WEB PAGE-ime.org.sg; "Tachyon and IME to Build 3D Chips for Greater Speed and Performance," Press Release, dated January 18, 2002			
	A126	ICHIRO FUJIWARA et al.: "MONOS Memory Cell Scalable to 0.1µm and Beyond," pages 117-118			

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